WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first transistor including a first gate formed on a semiconductor substrate, a first low impurity concentration diffusion layer formed on the surface of said semiconductor substrate in a manner to surround said first gate, a first high impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said first low impurity concentration diffusion layer, and a first gate side wall formed to surround the first gate; and

a second transistor including a second gate formed on the semiconductor substrate, a second low impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said second gate, a second high impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said second low impurity concentration diffusion layer, and a second gate side wall formed to surround said second gate and having a thickness equal to that of the first gate side wall of said first transistor;

wherein the size of said second low impurity concentration diffusion layer formed on the surface of the semiconductor substrate, which extends from said second gate to reach said second high impurity concentration diffusion layer, is larger than the size

of said first low impurity concentration diffusion layer formed on the surface of the semiconductor substrate, which extends from said second gate to reach said second high impurity concentration diffusion layer.

2. The semiconductor device according to claim 1, wherein said first low impurity concentration diffusion layer is an N-type diffusion layer having a low impurity concentration, said first high impurity concentration diffusion layer is an N-type diffusion layer having a high impurity concentration, said first transistor is an N-type transistor, said second low impurity concentration diffusion layer is a P-type diffusion layer having a low impurity concentration, said second low impurity concentration diffusion layer is a P-type diffusion layer having a low impurity concentration, and said second transistor is a P-type transistor.

3. The semiconductor device according to claim 2, further comprising a third N-type transistor and fourth P-type transistor, wherein said first and second transistors perform the function of a high voltage transistor, and said third and fourth transistors perform the function of a low voltage transistor.

4. The semiconductor device according to claim 1, further comprising a memory cell transistor including a third gate formed on said semiconductor substrate,

a third diffusion layer having a high impurity concentration and formed within said semiconductor substrate around said third gate, and third gate side wall formed around said third gate and having a thickness substantially equal to those of said first and second gate side walls.

5. The semiconductor device according to claim 3, further comprising a memory cell transistor including a third gate formed on said semiconductor substrate, a third diffusion layer having a high impurity concentration and formed within said semiconductor substrate around said third gate, and a third gate side wall formed around said third gate and having a thickness substantially equal to those of said first and second gate side walls.

6. The semiconductor device according to claim 5, wherein the third gate of said memory cell transistor includes a floating gate acting as a charge accumulating layer, a control gate formed above said floating gate, and an insulating layer interposed between said floating gate and said control gate.

7. The semiconductor device according to claim 5, wherein said memory cell transistor is a nonvolatile memory device, said first transistor is an N-type MOS transistor having a first LDD structure, and said second transistor is a P-type MOS transistor having a second LDD structure, said second LDD structure being

longer than said first LDD structure.

8. A method of manufacturing a semiconductor device, comprising:

forming a gate of a first transistor and a gate of a second transistor on a semiconductor substrate;

forming a first diffusion layer having a low impurity concentration in said semiconductor substrate with the gate of said first transistor used as a mask;

forming a second diffusion layer having a low impurity concentration in said semiconductor substrate with the gate of said second transistor used as a mask;

forming gate side walls of the same thickness to surround the gates of said first transistor and said second transistor, respectively;

forming a first diffusion layer having a high impurity concentration, which is positioned adjacent to said first diffusion layer having a low impurity concentration, within said semiconductor substrate, with the gate side wall of said first transistor used as a mask;

forming a mask side wall on the gate side wall of said second transistor;

forming a second diffusion layer having a high impurity concentration, which is positioned adjacent to said second diffusion layer having a low impurity concentration, within said semiconductor substrate, with the mask side wall used as a mask; and

removing said mask side wall.

9. The method of manufacturing a semiconductor device according to claim 8, wherein said first diffusion layer having a low impurity concentration is an N-type diffusion layer having a low impurity concentration, said first diffusion layer having a high impurity concentration is an N-type diffusion layer having a high impurity concentration, said first transistor is an N-type transistor, said second diffusion layer having a low impurity concentration is a P-type diffusion layer having a low impurity concentration, said second diffusion layer having a low impurity concentration is a P-type diffusion layer having a high impurity concentration, and said second transistor is a P-type transistor.

10. The method of manufacturing a semiconductor device according to claim 8, further comprising:

forming a third gate of the memory cell transistor on said semiconductor substrate;

forming a third diffusion layer having a high impurity concentration within said semiconductor substrate around said third gate; and

forming a third gate side wall substantially equal in thickness to said first and second gate side walls around said third gate.

11. The method of manufacturing a semiconductor device according to claim 9, wherein a floating gate

acting as a charge accumulating layer, a control gate positioned above said floating gate, and an insulating layer interposed between said floating gate and said control gate are formed as a third gate of said memory cell transistor.

12. The method of manufacturing a semiconductor device according to claim 8, wherein said memory cell transistor is a nonvolatile memory device, said first transistor is an N-type MOS transistor having a first LDD structure, and said second transistor is a P-type MOS transistor having a second LDD structure, said second LDD structure being longer than said first LDD structure.

13. A method of manufacturing a semiconductor device according to claim 8, comprising:

forming on the semiconductor substrate a gate of a high voltage PMOS transistor as said second transistor and a gate of a high voltage NMOS transistor as said first transistor;

forming an N^- diffusion layer within said semiconductor substrate with the gate of said high voltage NMOS transistor used as a mask;

forming said gate side walls substantially equal to each other in thickness on the gates of said high voltage PMOS transistor and said high voltage NMOS transistor;

forming an N^+ diffusion layer within said

semiconductor substrate with the gate side wall of said high voltage NMOS transistor used as a mask;

forming an P^- diffusion layer within said semiconductor substrate with the gate side wall of said high voltage PMOS transistor used as a mask;

forming said mask side walls substantially equal to each other in thickness on the first side walls of said high voltage PMOS transistor and said high voltage NMOS transistor; and

forming a P^+ diffusion layer within said semiconductor substrate by using the mask side wall of said high voltage PMOS transistor.

14. A method of manufacturing a semiconductor device, comprising:

forming a first gate insulating film for a high voltage transistor on a semiconductor substrate;

forming a second gate insulating film for a low voltage transistor, said second gate insulating film being thinner than said first gate insulating film;

forming a stacked gate structure by stacking conductive materials forming the gate electrode, followed by selectively patterning by etching the stacked structure;

introducing an impurity of a first conductivity type into the semiconductor substrate;

depositing a first side wall material;

forming a first side wall on the side surface of

said gate electrode by selectively etching said first side wall material by means of an anisotropic etching;

introducing an impurity into a fist MOS transistor region of the semiconductor substrate in a concentration higher than that in an impurity diffusion layer of a second conductivity type;

depositing a second side wall material and a third side wall material differing from said second side wall material;

forming a third side wall on the side surface of said second side wall by selectively etching said third side wall material by means of an anisotropic etching;

introducing an impurity of said first conductivity type into the second MOS transistor region of the semiconductor substrate with said third side wall used as a mask;

depositing an interlayer insulating film on the entire surface of said semiconductor substrate; and

selectively forming contact holes in said interlayer insulating film.

15. A method of manufacturing a semiconductor device, comprising:

forming an element isolating region in a semiconductor substrate;

forming a tunnel oxide film for a memory cell, a floating gate and an interlayer insulating film;

forming a first gate insulating film for a high

voltage transistor on said semiconductor substrate;

forming a second gate insulating film for a low voltage transistor, said second gate insulating film being thinner than said first gate insulating film;

stacking conductive materials forming a control gate and a floating gate, followed by selectively patterning successively said control gate, said interlayer insulating film, and said floating gate;

selectively patterning the gate electrode in the peripheral circuit region;

introducing an impurity of a second conductivity type into the semiconductor substrate in the memory cell region and the peripheral circuit region;

depositing a first side wall material;

forming a first side wall on the side surface of said gate electrode by selectively etching the first side wall material by an anisotropic etching;

introducing an impurity into the first MOS transistor region of the semiconductor substrate in a concentration higher than that in said impurity diffusion layer of the second conductivity type;

depositing a second side wall material and a third side wall material differing from said second side wall material;

forming a third side wall on the side surface of said second side wall by selectively etching said third side wall material by an anisotropic etching;

introducing an impurity of a first conductivity type into a second MOS transistor region of said semiconductor substrate with said third side wall used as a mask;

removing said third side wall;

depositing an interlayer insulating film on the entire surface of said semiconductor substrate;

selectively forming contact holes in said interlayer insulating film;

forming a metal wiring; and

forming an insulating film on said metal wiring.

16. A method of manufacturing a semiconductor device, comprising:

forming an element isolating region in a semiconductor substrate;

forming a first gate insulating film for a high voltage transistor on said semiconductor substrate;

forming a second gate insulating film for a low voltage transistor, said second gate insulating film being thinner than said first gate insulating film;

stacking a conductive material layer forming a gate electrode, followed by pattering said conductive material layer by an etching;

introducing an impurity of a second conductivity type into a first MOS transistor region of the semiconductor substrate;

depositing a first side wall material;

forming a first side wall on the side surface of said gate electrode by selectively etching said first side wall material by an anisotropic etching;

introducing an impurity of a first conductivity type into a second MOS transistor region of the semiconductor substrate with said first side wall used as a mask;

introducing an impurity into the first MOS transistor region of the semiconductor substrate in a concentration higher than that in the diffusion layer of the second conductivity type;

depositing a second side wall material and a third side wall material differing from said second side wall material;

forming a third side wall on the side surface of said second side wall by selectively etching said third side wall material layer by an anisotropic etching;

introducing an impurity of the first conductivity type into a second MOS transistor region of the semiconductor substrate in a concentration higher than that in the impurity diffusion layer of the first conductivity type;

removing the third side wall;

depositing an interlayer insulating film on the entire substrate; and

selectively forming contact holes in said interlayer insulating film.

17. The method of manufacturing a semiconductor device according to claim 16, further comprising:

forming on said semiconductor substrate an element isolating region, a tunnel oxide film for a memory cell device, a floating gate electrode for said memory cell device and an interlayer insulating film for said memory cell device;

forming at least a single layer of a metal wiring on said contact hole; and

forming an insulating film on said metal wiring.

18. A method of manufacturing a semiconductor device, comprising:

introducing an impurity of a first conductivity type into a semiconductor substrate;

forming a tunnel oxide film and a floating gate in a memory cell region;

forming a first gate insulating film for a high voltage transistor in a peripheral circuit region;

forming a second gate insulating film for a low voltage transistor, said second gate insulating film being thinner than said first gate insulating film;

forming an interlayer insulating film for a memory cell;

stacking conductive materials forming a control gate and a floating gate, followed by selectively patterning by etching said control gate, said interlayer insulating film, and said floating gate

successively;

selectively patterning the gate electrode of a peripheral circuit region;

introducing an impurity of a second conductivity type into the memory cell region and the first MOS transistor region included in the peripheral circuit of the semiconductor substrate;

depositing a first side wall material;

forming a first side wall on the side surface of said gate electrode by selectively etching said first side wall material layer by an anisotropic etching;

introducing an impurity of a first conductivity type into the second MOS transistor region of the semiconductor substrate;

introducing an impurity into the first MOS transistor region of the semiconductor substrate in a concentration higher than that in the impurity diffusion layer of the second conductivity type;

depositing a second side wall material and a third side wall material differing from said second side wall material;

forming a third side wall on the side surface of the second side wall by selectively etching said third side wall material by an anisotropic etching;

introducing an impurity into the second MOS transistor region of the semiconductor substrate in a concentration higher than that in said impurity

diffusion layer of the first conductivity type;

removing said third side wall;

depositing an interlayer insulating film on the entire surface of the substrate;

selectively forming contact holes in said interlayer insulating film;

forming at least a single metal wiring; and

forming an insulating film on said metal wiring.